IDS # 3

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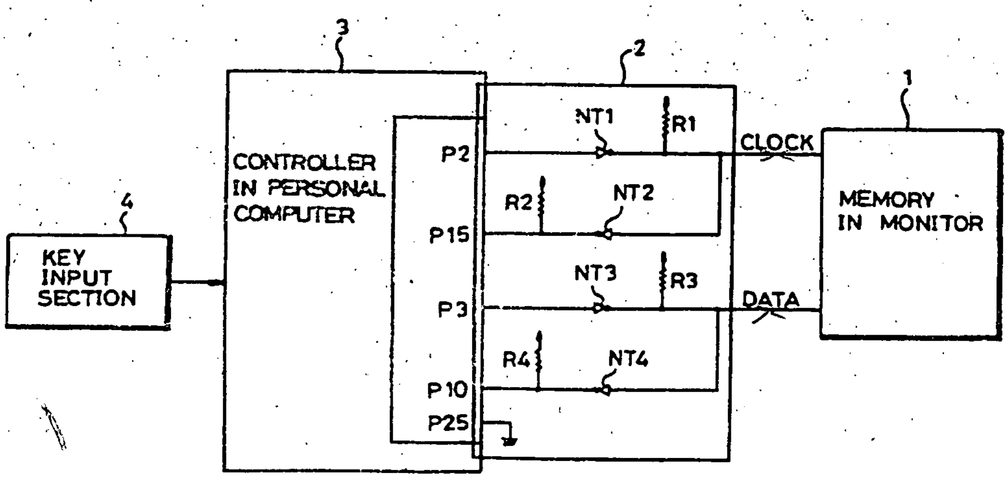
(54) Monitor communicates with computer via serial peripheral interface

(57) Picture adjustment data for the monitor is written to or read from the memory 1 built into the monitor by the computer. The written or read data may be displayed.

An interface 2, that may be coupled to a serial peripheral port of the computer, e.g the printer port, has a clock line and a data line coupled between the computer and the memory of the monitor.

The computer controls the data to and from the memory by serial peripheral interface communication (SPI).

FIG. 1



PC reads & writes data from and to monitor via serial peripheral interface SPI
or DDC

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FIG. 1

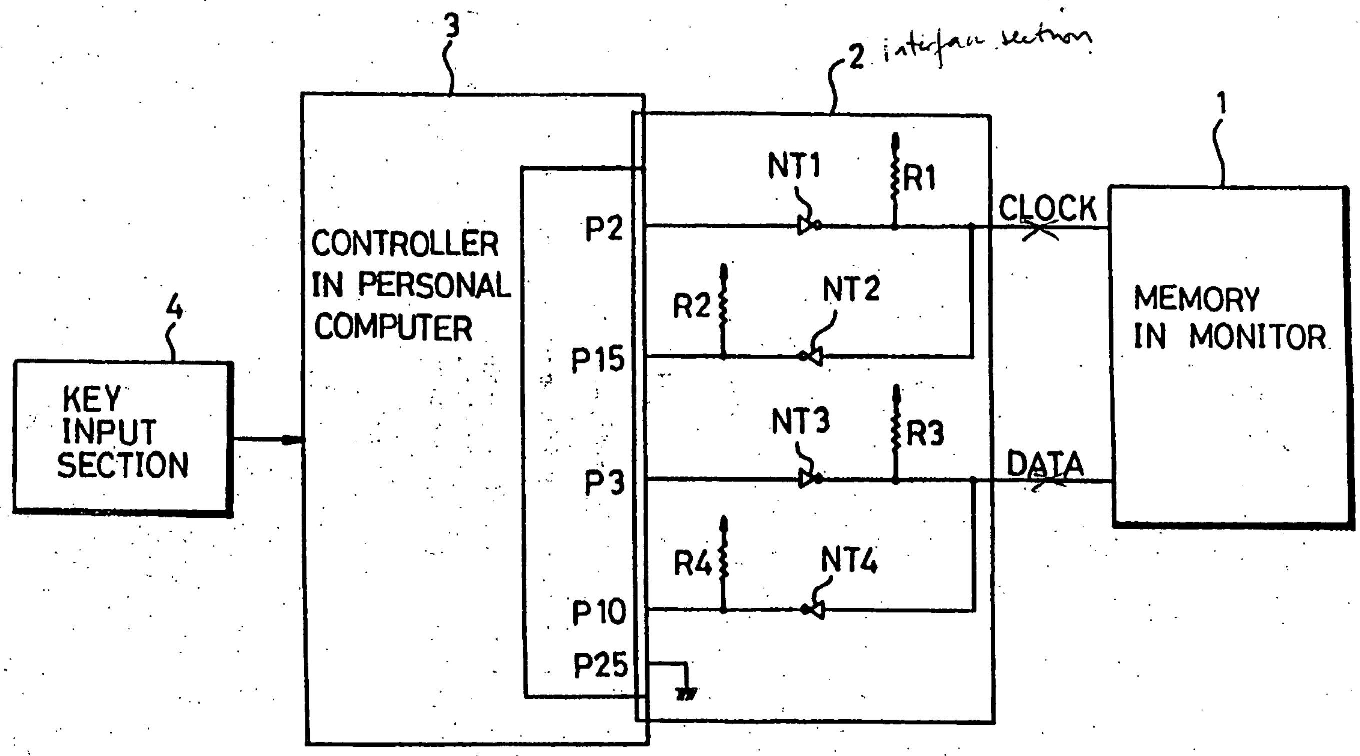
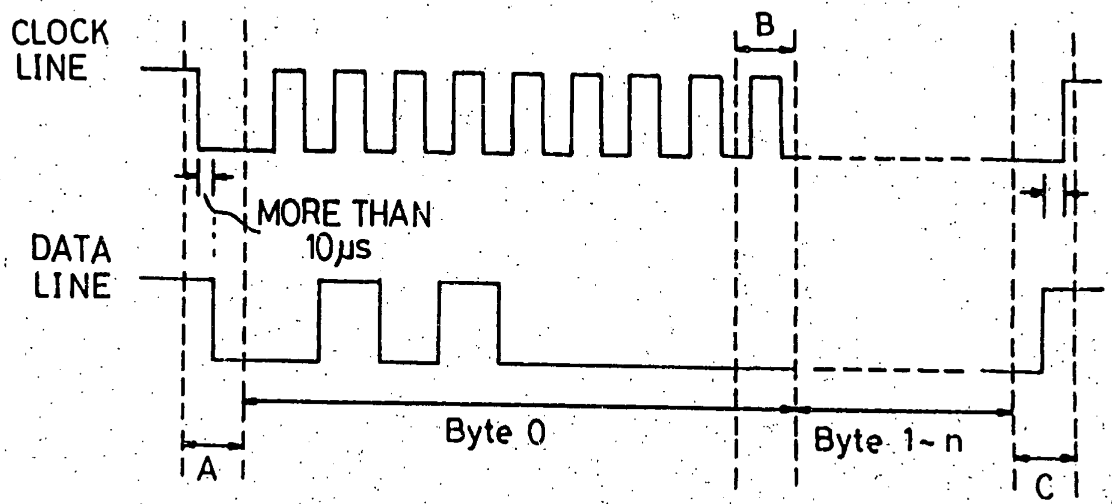

1
MEMORY IN MONITOR
2 interface section
CLOCK
DATA
NT1
NT2
NT3
NT4
R1
R2
R3
R4
P2
P15
P3
P10
P25
3
CONTROLLER IN PERSONAL COMPUTER
4
KEY INPUT SECTION

FIG. 2A

FIG. 2B



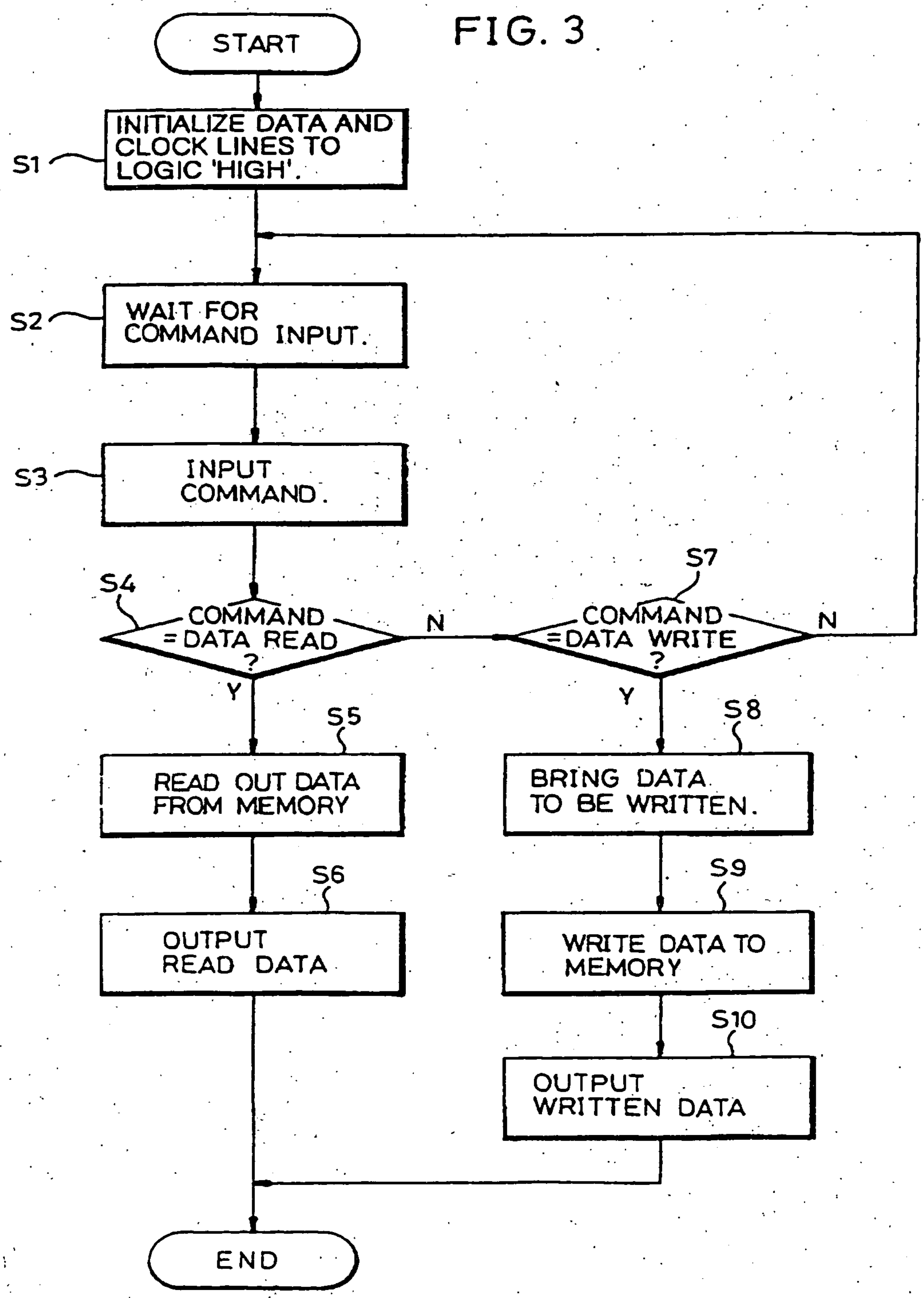

START
S1
INITIALIZE DATA AND CLOCK LINES TO LOGIC 'HIGH'.
S2
WAIT FOR COMMAND INPUT.
S3
INPUT COMMAND.
S4
COMMAND =DATA READ ?
N
Y
S5
READ OUT DATA FROM MEMORY
S6
OUTPUT READ DATA
S7
COMMAND =DATA WRITE ?
N
Y
S8
BRING DATA TO BE WRITTEN.
S9
WRITE DATA TO MEMORY
S10
OUTPUT WRITTEN DATA
END

FIG. 3

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MONITOR COMMUNICABLE WITH PERSONAL COMPUTER

The present invention relates to a monitor which is communicable with a personal computer (PC). In particular, the present invention relates to a monitor communicable with a PC, whereby data for controlling a picture display state of the monitor can be written in or read out from a memory provided in the monitor utilizing the PC by implementing an interface between the PC and the memory in the monitor.

Generally, variable resistors have been used in adjusting or controlling the contrast, brightness, horizontal and vertical pulses of the monitor. Recently, a monitor which has a built-in microcomputer for controlling the picture display state of the monitor has been in commercial use. In such a monitor, the picture display state is controlled utilizing control buttons provided on the exterior of the monitor. Also, a panel of light emitting diodes (LEDs) or a liquid crystal display (LCD) is attached to the exterior of the monitor, and thus the input state of control signals for controlling the contrast, brightness, horizontal and vertical pulses and the picture display state being controlled by the control signals are displayed on the panel for convenience in use.

A monitor having an interface between a microcomputer inside the monitor and a PC has been disclosed. On this monitor the picture display state of the monitor, which is controlled by the microcomputer, can be directly displayed on the

screen of the monitor utilizing a keyboard of the PC. Accordingly, it is not required to attach an LCD or LED panel, as well as control buttons, to the exterior of the monitor.

However, the conventional monitor communicable with a PC has the drawback that the adjustment or control of the display is not possible, but the information on the display state is displayed on the screen only, enabling the user to recognize the adjusted display state.

It is an object of the present invention to solve the problems involved in the related art, and to provide a monitor communicable with a PC, whereby data stored in a memory provided in the monitor is read out or data is written in the memory utilizing the PC by implementing an interface between the memory and the PC.

In order to achieve the above object, there is provided a monitor communicable with a PC, having preferably a serial peripheral interface (SPI) communication type memory, the monitor comprising an interface provided between the PC and the monitor and having a clock line and a data line, wherein the PC writes data in the memory or reads out the data from the memory through the interface.

The above object, other features and advantages of the present invention will become more apparent by describing the preferred embodiment thereof with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram of the monitor communicable with a PC according to the present invention;

FIGS. 2A and 2B are waveform diagrams illustrating a clock signal and data on a clock line and a data line for SPI communication according to the present invention; and

FIG. 3 is a flow chart illustrating the data read/write operation according to the present invention.

Referring to FIG. 1, a memory 1 utilizing SPI communication is installed inside the monitor. An interface section 2 having a clock line and a data line is coupled between an I/O port such as a printer port of a controller 3 in the PC and the memory 1 in the monitor. The controller 3 in the PC reads out data stored in the memory in the monitor or writes the data to the memory 1 through the clock and data lines in accordance with the input of a communication mode determining key and a data read/write key inputted through a key input section 4.

Specifically, the interface section 2 includes a first inverter NT1, connected to a printer port pin P2 of the controller 3, for inverting a clock signal outputted from the printer port pin P2 for the control of its clock line. A second inverter NT2 feeds back the clock signal which is transferred to the memory 1 through the inverter NT1 to a printer port pin P15 so that the controller 3 can check the state of the clock line. A third inverter NT3, connected to a printer port pin P3 of the controller 3, inverts data outputted from the printer port P3 for the control of its data line. A fourth inverter NT4 feeds back the data which is transferred to the

memory 1 through the inverter NT3 to a printer port pin P10 so that the controller 3 can check the state of the data line. In Fig.1, the numerals R1 to R4 denote pull-up resistors.

The operation of the monitor communicable with the PC according to the present invention as constructed above will now be explained with reference to FIGs. 1, 2A, 2B and 3.

The data for the picture adjustment of the monitor is written to or read out from the memory 1 in the monitor utilizing the SPI communication by the PC. The written or read out data is displayed on the screen of the monitor.

Referring to FIG. 1, in order to read out or write data through the clock line and the data line of the interface section 2, the memory 1 in the monitor is coupled to the controller 3 in the PC. Specifically, the printer port pins P2 and P3 are coupled to the memory 1 in the monitor via the interface section 2.

First, in order to perform communication between the PC and the monitor, the controller 3 in the PC initializes the data line and the clock line of the interface section 2 by switching them to a logic 'high' level (step S1 of FIG. 3) in accordance with the communication mode key signal inputted through the key input section 4, and waits for the key input for the data read/write (step S2 of FIG. 3).

Thereafter, if the key signal for writing the data to the

memory 1 or for reading out the data stored in the memory 1 is inputted (step S3 of FIG. 3), the controller 3 determines whether the inputted key signal corresponds to the data read command or the data write command (step S4 of FIG. 3), and produces a start condition for data communication to execute the corresponding routines, respectively.

The start condition is given in a manner that the controller 3 first switches the clock line to a logic 'low' state, and after a predetermined time (for example more than 10μs) elapses the controller 3 switches the data line to a logic 'low' level as shown within the period "A" in FIGs. 2A and 2B.

If the key signal for writing the data in the memory 1 is inputted, the controller 3 transfers to and writes in the memory 1 the clock signal and the data through the inverters NT1 and NT3 in the interface section 2 (steps S8 and S9 of FIG. 3). At this time, the clock signal and the data outputted through the inverters NT1 and NT3 are also fed back to the controller 3 through the inverters NT2 and NT4, respectively, and thus the controller 3 checks if the clock signal and the data are normally outputted through the clock line and the data line. Then, the controller 3 writes the data in the memory 1, and displays the contents of the data written in the memory 1 on the screen of the monitor as well (step S10 of FIG. 3).

If the key signal is to read out the data stored in the memory 1, the controller 3 outputs the clock signal to the memory 1 through the inverter NT1, and then receives the data, which is read out from the memory 1 in response to the clock signal, through the inverter NT4 (step S5 of FIG. 3). At this time, the controller 3 also displays the contents of the data read

out from the memory 1 on the screen of the monitor (step S6 of FIG. 3).

If the 9th clock is inputted or outputted through the clock line as the data communication is performed between the controller 3 in the PC and the memory 1 in the monitor as described above, i.e. if the clock signal goes to a 'high' level nine times after the start condition is produced, the controller 3 recognizes that transmission/reception of one byte of data is completed as shown within the period "B" in FIGs. 2A and 2B. By repeating the above-described operation, data transmission/reception byte by byte is performed between the controller 3 and the memory 1. At this time, the data which is read out from or written to the memory 1 is displayed on the screen of the monitor by the controller 3. As can be appreciated the present invention allows a user to conveniently control the display state of the monitor through the personal computer without having to play with the external control switches and buttons of the monitor.

If the data read/write operation as above is completed, the controller 3 produces a stop condition for terminating the data read/write operation as shown in the period "C" in FIGs. 2A and 2B.

For example, in the event that the controller 3 in the PC writes data in the memory 1 to the monitor, the controller 3, in order to transmit the data by SPI communication, controls the state of the printer port pins P2 and P3 so that the signals as shown in FIGs. 2A and 2B are provided through the clock line and the data line.

Specifically, if the clock line is to be in a logic 'low' state, the output of the printer port pin P2 goes to a logic

'high', while if the clock line is to be in a logic 'high' state, the output of the printer port pin P2 goes to a logic 'low'. The state of the data line is controlled in the same manner as that of the clock line.

As a result, the user can write data in the memory 1 of the monitor or read-out the data stored in the memory 1 utilizing a PC. The read out or written data is also displayed on the screen of the monitor for convenience in use.

As described above, according to the present invention, SPI communication is achieved between a PC and a monitor using an SPI communication type memory by constructing an interface between the PC and the monitor. Accordingly, data can be read out from or written to the memory without separating the memory from a printed circuit board of the monitor.

While the present invention has been described and illustrated herein with reference to the preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention.

CLAIMS:

1. A monitor having a memory communicable with a personal computer (PC), comprising an interface coupled to the memory and arranged to be communicably coupled to the PC, the interface having a clock line and a data line, wherein the writing of data to the memory or reading of data from the memory is controllable by the PC by a serial peripheral interface communication through the interface.

2. A monitor as claimed in claim 1, wherein the data includes data for adjusting at least one picture display state of the monitor, such as contrast, brightness, horizontal and vertical pulses.

3. A monitor as claimed in claim 1 or 2, further comprising key input means operably connected with the PC, the input means including a communication mode key for establishing a communication mode, a data read/write determining key, and numeral keys for inputting data values for writing the data.

4. A monitor as claimed in claim 1, 2 or 3, wherein the monitor is responsive to the PC to control a display of the data on a screen of the monitor during reading/writing of the data..

5. A monitor as claimed in any of claims 1 to 4, wherein the interface comprises a plurality of inverters for inverting the clock signal, and the data being communicated between the PC and the monitor through the clock line and data line, and for feeding back to the PC the clock signal and the data being transferred to the

memory so that the PC checks the state of the clock line and the data line.

6. A system comprising:

a personal computer (PC);

a monitor having a memory communicable with the PC;

key input means connected to the PC and including a communication mode key for establishing a communication mode, a data read/write determining key, and numeral keys for inputting data values;

a controller in the PC, for performing serial peripheral interface communication with the memory in accordance with key signals inputted thereto through the key input means; and

an interface, coupled between the controller and the memory and having a clock line and a data line, for interfacing between the controller and the memory so that the controller writes the data to the memory or reads out the data stored in the memory.

7. A system as claimed in claim 6, wherein the data includes data for adjusting a picture display state of the monitor such as contrast, brightness, horizontal and vertical pulses.

8. A system as claimed in claim 6, wherein the PC controls to display of the data on a screen of the monitor during reading/writing of the data.

9. A system as claimed in claim 6, wherein the interface comprises a plurality of inverters for inverting the clock signal and the data being communicated between the PC and the monitor through the clock line and the data line, and for feeding back to the

PC the clock signal and the data being transferred to the memory, the PC being arranged to check the state of the clock line and the data line from the feedback signals.